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INTERFACE OF THE TRANSPORT SYSTEMS RESEARCH VEHICLE
MONOCHROME FLIGHT DISPLAY SYSTEM TO THE DIGITAL
AUTONOMOUS TERMINAL ACCESS COMMUNICATION DATA BUS

Wesley C. Easley and John S. Tanguy

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National Aeronautics and
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Langley Research Center
Hampton, Virginia 23665



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Summary

The technical effort described in this report was performed to interface the original TRANSPORT SYSTEMS RESEARCH VEHICLE (TSRV) monochrome display system (ADVANCED ELECTRONIC DISPLAY SYSTEM (ADEDS)) to the new Digital Autonomous Terminal Access Communication (DATAC) bus which was chosen for use in an upgrade of the TSRV experimental system. The ADEDS is a unique prototype system for which complete documentation was never prepared. Modifications are very difficult. Thus it was decided to leave it unchanged and design a unique interface to the new DATAC data bus system. The new interface is designated as the Display Interface Unit (DIU).

A Shared Interface Random Access Memory (SIR) is used in the DATAC bus system as an intermediate storage medium for data transferred via the bus. The ADEDS-to-DATAC interface (the DISPLAY INTERFACE UNIT) described in this report functions by reading data from and writing data to this SIR.

Input data to the ADEDS consists of three serial busses using Split Phase Bipolar (SPBP) modulation. The DIU was designed to read display input data from the SIR and transfer it via a parallel bus to internal latches. Then internal DIU conversion circuitry is activated which transfers the latched data serially into SPBP transmitters which in turn modulate the data bits onto the SPBP waveform and send them to the ADEDS input buffers.

Another SPBP bus is present in the ADEDS for transfer of pilot selected display functions to the computer system. This data is handled by the DIU in the reverse manner. It accepts the serial SPBP input data, places it into parallel latches, and writes it into the SIR for return via the DATAC bus to the host computer.

Data for each SPBP bus is written into designated SIR locations. Timing signals are generated in the DIU to insure frame synchronization of all data.

The application described in this report is important because it is an example of interfacing existing avionics to an advanced bus concept.

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INTRODUCTION

A major aspect of the ADVANCED TRANSPORT OPERATING SYSTEM TRANSPORT SYSTEMS RESEARCH VEHICLE upgrade was the implementation of the Digital Autonomous Terminal Access Communication (DATAC) data bus system recently developed by the Boeing Commercial Airplane Company (Ref. 1). DATAC is a high-speed (1 megabit per second) serial data bus which effects digital data transfer among a number of terminals inductively coupled to the bus.

Use of the DATAC bus in the TSRV upgrade structure is illustrated in Figure 1. Two DATAC busses are used: one, the Global Bus, handles data communication involving the two Norden 11/70 computers and the sensor interface units; the second, the Display Bus, handles communication between the display host Norden 11/70 and the flight display system.

The initial TSRV upgrade retained the monochrome display system. Due to its unique design and very limited suitability for modification it was left unchanged. This created a requirement for development of a technique for extracting data from the new DATAC bus and converting it into a form suitable for use by the existing system.

This interfacing requirement was met by the in-house design, fabrication, testing, and implementation of the DISPLAY INTERFACE UNIT (DIU) which is the subject of this report.

LIST OF ABBREVIATIONS

| | |
|---------|--|
| AEDDS | Advanced Electronic Display System |
| ATOPS | Advanced Transport Operating System |
| DATA C | Digital Autonomous Terminal Access Communication |
| DIU | Display Interface Unit |
| EPROM | Eraseable Programmable Read Only Memory |
| GS | Glide Slope |
| H | Hexadecimal Number |
| ILS | Instrument Landing System |
| INS | Inertial Navigation System |
| LOC | Localizer |
| LSB | Least Significant Bit |
| Mhz | Megahertz |
| MS | Millisecond |
| MSB | Most Significant Bit |
| RAD ALT | Radio Altitude |
| RAM | Random Access Memory |
| RTN | Return |
| SIR | Shared Interface RAM |
| SPBP | Split Phase Bipolar (Data Modulation) |
| SYNC | Synchronization |
| TCV | Terminal Configured Vehicle |
| TSRV | Transport Systems Research Vehicle |
| TTL | Transistor-Transistor Logic |

DISPLAY SYSTEM DATA INTERFACE REQUIREMENTS

Figure 2 illustrates the data interface requirements of the monochrome display system. The signals shown on the right are direct inputs from aircraft sensors and were not changed as part of the upgrade. The signals shown on the left represent display-host communication data that must be transferred by the DATAC bus system. Reference 2 describes the operational aspects of the display system.

Data Signal Type:

The four signal lines shown on the left represent split phase bipolar (SPBP) data busses. SPBP is a 50-kilobit-per-second serial data bus type that was used rather extensively in the previous TSRV experimental system. Figure 3 illustrates the SPBP transmission line waveform and data modulation method. Figure 4 illustrates the digital structure of each SPBP data word. It is seen that each word consists of 32 bits with the least significant 8 bits constituting an address label.

Data Functions:

The three input busses shown on the left in figure 2 contain display instruction information produced by host computer processing of sensor data. Using this input instruction data the display processor produces real-time navigation and attitude displays for use by the research pilots. Bus 1 consists of data blocks containing 512 SPBP words (32 bits each) of map background data, and a block is transmitted at a rate not faster than once per second. Busses 2 and 3 are each composed of 64 SPBP word data blocks with blocks transmitted at a rate not slower than once every 100 ms. They provide fast changing position data for the background symbols controlled by Bus 1 data. The return bus transmits display status information and pilot mode panel selections back to the host computer. It consists of, at most, 8 SPBP words and is transmitted each 50 ms frame.

Data Timing:

Figure 5 shows the display system timing requirements for data supplied by the three SPBP busses. Due to computational time limitations in the display processor, only two of the three busses may be active simultaneously in any data frame. The large quantity of data on Bus 1 results in a time requirement of approximately eight 50 ms frames for one transmission. While bus 1 is transmitting, busses 2 and 3 are active during alternate 50 ms frames; and while bus 1 is inactive, busses 2 and 3 are transmitted simultaneously each frame.

NEW INTERFACE IMPLEMENTATION

Functional Requirements:

Previously a Litton C-4000 host computer performed the task of configuring the three display input SPBP busses using aircraft sensor data and status data from the display system. Direct SPBP transmitter/receiver links existed between the C-4000 and the display computer. However, with the change to the Norden 11/70 host computer, the interfacing is altogether different. Software in the Norden host still configures the data for each display input bus and determines which two busses are to be active each frame, but the Norden cannot handle SPBP data links. With the use of the DATAC/Norden interface (figure 1), data words for all busses are in fact transmitted to and from the host at different times during a frame. Since the display system was not changed, a requirement existed for a method of emulating the C-4000/display system interface using display data transferred via the serial bidirectional DATAC bus.

Implementation Concept:

The general implementation concept is illustrated in the top portion of figure 1. Display data is transferred via the dedicated display DATAC bus between a terminal interfacing with the host and a terminal interfacing with the DIU. Each terminal contains a Shared Interface RAM (SIR) which is a 4K-word by 16-bit-buffer memory used for temporary storage of data transferred via DATAC. The Display Interface Unit (DIU) reads display input data from the SIR, routes it to the proper SPBP bus data latches, and sends it via its internal SPBP transmitters to the display processor. Return data is handled in reverse; the DIU receives the display system SPBP output data, reformats it, and writes it into proper SIR locations for return transmission to the host.

Bus Data Separation:

The method of separating display data for each bus is illustrated in figure 6, which is a SIR memory map for the DATAC terminal interfacing with the DIU. Data transmitted by the DATAC bus is identified by user chosen labels. Firmware in the terminals is used to decode the labels and route data to its assigned SIR locations. Specific labels and SIR locations are configured for each SPBP bus as well as for the display bus control word which is described below in the section on synchronization. Bus 1 contains 512 32-bit SPBP words; hence, Bus 1 data occupies 1024 locations in the 16-bit SIR. Busses 2 and 3 each contain 64 SPBP words, or 128 SIR locations. The display return data is allocated 16 SIR locations, only 6 of which are presently in use (3 SPBP words). The bus control word occupies only one location, 0600H.

Synchronization of Host and Display System Data Transfer:

Two problems required solution in the design of the display/Norden data communication link to insure proper frame registration of data transferred

between the host and the display system. They were: (1) insuring that the proper SPRP data busses are active for a given frame, and (2) insuring that a frame of display data is not used until it has settled in the SIR.

The synchronization method used is illustrated in figures 7 and 8. Bus selection is accomplished by a bus control word, the structure of which is shown in figure 7. This word is configured every frame in host software, transmitted via DATAC along with the frame's active data, and written into SIR location 0600H. The 3 least significant bits are used for bus control; bit 0 for bus 1, bit 1 for bus 2, and bit 2 for bus 3. A one (bit set condition) in any of these bits means that its corresponding bus is to be used that frame; a zero (bit reset condition) means the corresponding bus is off for that frame. Only two of the three bits may be set for any one frame.

The other important synchronization consideration results from the fact that a certain amount of time (typically a few nanoseconds) is required for settling and stabilization of the data in the SIR after DATAC transmission. To signify that SIR data is ready for use, a frame sync pulse is generated by the DATAC terminal each 50 ms frame for each bus. These pulses are firmware controlled interrupt vectors whose delay time is user programmable.

Figure 8 contains an illustration of the specific method by which the bus control word and the frame sync pulses control data transmission to the display system. In the DIU the DATAC frame sync pulses and logic states generated from the pertinent bus control word bits are used as inputs to an AND gate. This means that the DIU address counters will not start until both these signals are active (AND gate is enabled). Since starting the DIU address counters is the mechanism used to trigger SPRP data transmission to the display system, the result is that this data transmission is simultaneously slaved to both the host and the DATAC bus system. Once an address counter is started, it will automatically step through the entire SIR buffer area assigned to its corresponding bus, then reset itself and wait for the trigger logic of figure 8 to again occur. More detailed discussion of the DIU inner workings is contained in following paragraphs.

The return data does not require exact frame time registration and is handled in a slightly different manner. It consists of mode panel data which is stored in latches in the DIU and transmitted routinely each frame. The mode panel data changes only upon manual input from the display pilot mode select panels, and its entry is thus asynchronous. New mode panel data will be transferred by the DIU to the SIR during the first full frame after it is present in the DIU data latches. Thus, there can be a frame time delay after selection before the data is transferred into SIR memory. This is satisfactory since the host software does not assure updated information using the new return data in less than one second. A 50 ms frame time delay in transmission therefore goes unnoticed.

DISPLAY INTERFACE UNIT (DIU) TECHNICAL DESCRIPTION

The remaining sections of this report contain a technical description of the DIU.

Overall Operational Functions:

As previously stated, the DIU functions are: (1) read host-generated display input data from SIR locations, reformat the data, and transmit it serially via internal SPBP transmitters to the display system, and (2) receive SPRP data from the display system, reformat this data, and write it into proper SIR locations for transmission via the DATAC bus to the host. Figure 9 is a functional diagram of the DIU.

Address Selection Circuitry for Data Reading:

Selection of the address to be read is accomplished by the address counters and the address latches as illustrated in figure 9 and in more detail in figure 10. A DIU address counter exists for each of the three input busses. Each counter consists of a series of 54LS193 chips configured such that the initial value on the address select lines is the starting location in SIR of the buffer area containing data for its corresponding bus. Examination of figure 6 shows that the Bus 1 counter is initially set to 0000H, Bus 2 to 0400H, and Bus 3 to 0480H. At all times the 12 lines from each address counter present a 12-bit address value to its latches which are in turn connected to the DIU/DATAC address bus. Upon receipt of the proper timing pulses (discussed below) an address counter's latches are enabled thus presenting its selected address value to the SIR. This constitutes a request to the SIR to provide the data from that location onto the DIU/DATAC data bus.

Data Read Circuitry:

Once the SIR receives the read request described in the previous paragraph, it responds by enabling latches such that the data from the requested location is present on the DIU/DATAC data bus and ready for use. Then upon receipt of a properly timed pulse (described in detail below), the DIU data latches (figures 9 and 10) are enabled, thus capturing the data hits on the line at that precise time. With this event the DIU has possession of the data from the location it requested and proceeds by means of internal circuitry to transfer it to the proper SPBP transmitter input which in turn sends it serially out to the display system. A separate SPRP transmitter exists for each bus.

Address Counter Cycling:

After the data from a SIR location has been captured by the DIU data latches as described above, the address and data busses are available for use in reading data from the next location of the buffer being used. This is done by stepping the counter by one thus presenting the next address value to the DIU address latches and hence to the SIR and repeating the data read cycle. The pulse to increment the address counter is the STEP COUNTER input shown in

figure 10. It is generated by DIU timing circuitry to be discussed below. Each address counter is hardwired so that it will not increment above the last SIR address containing data for its corresponding bus. Bus 1 counts through SIR location 03FFH (1024 steps), Bus 2 counts through location 047FH (128 steps), and Bus 3 counts through location 04FFH (128 steps). When the maximum count is reached, the counter generates its own reset pulse and returns to its initial value. It will not restart until receipt of proper sync control pulses which have been described previously. (See figure 8.) These sync control pulses produce the START COUNTER input shown in the upper left of figure 10.

Bus Control Word Reading:

The bus control word (SIR location 0600H) contains 3 bits which are used as part of frame synchronization. Therefore this word must be read at the beginning of each frame so that the DATAC frame sync pulses will trigger only the bus address counters selected by host computer software. To accomplish this, the DIU was designed so that the default value on the address bus is 0600H. This means that in the absence of any other selected address, location 0600H will be continuously read and its data will be present in the DIU data latches. Thus, unlike any other SIR location, no frame sync pulse is required for reading this location. As has been stated, the bus control word is updated by the host at the beginning of each frame. The frame sync pulses are delayed slightly beyond the frame start time to allow for data settling in the SIR. Thus the inputs to the AND gates of figure 8 which result from bus control word bits will be configured before arrival of the frame sync pulses. This insures that no counter will be started by a frame sync pulse unless the host software has selected it for the frame in question.

DIU Write Address Selection:

The DIU must write the return words into proper SIR locations for transmission via DATAC back to the host. Only 3 SPRP words (12 SIR locations) are used. No address counter exists in the DIU for selection of these return word addresses as was the case for data reading. Instead, use is made of the address label contained in the least significant 8 bits of each SPRP word received from the display computer. Figure 4 illustrates the SPRP word structure and shows the location of the address label bits.

The return words to be written into SIR enter the DIU by means of its SPRP receiver. Examination of figure 10 shows that the output of this receiver is directed to both the data latch and the address latch, the latter via address label strip logic. The address label strip logic collects the least significant 8 bits of the received word and directs these bits to the address latches. These label bits are then added to a preset bias of 0500H in the return word address selection logic to form the SIR location to which the word in question is to be written. The specific return words used have address labels (generated by the display computer) of 00H, 04H, and 08H.

Thus the address label strip logic yields return word SIR locations of 0500H, 0540H, and 0580H. However, it is seen from figure 4 that 24 data bits remain in each SPRP word after the label is gone. This cannot be contained in one 16-bit SIR location; hence each address label must control 2 SIR locations. This is done in the return word address selection logic (figure 10) by incrementing the SIR address value after the first 16 bits of the data word are placed into the data latch. The remaining 8 bits are written into the least significant byte of the next highest SIR location. The upper byte of this location will thus contain unused data bits. The final result is the following SIR locations for the 3 return SPRP words: word 1 is in locations 0500H and 0501H, word 2 is in locations 0540H and 0541H, and word 3 is in locations 0580H and 0581H.

Data Transfer Timing:

The previous several paragraphs describe the electronic signal flow involved in the DIU/SIR data transfer. The next topic is timing requirements for controlling these data transfer signals. There is only one address bus and one data bus in the DIU; yet data for three separate input data busses and one output data bus must be transferred during each data frame. All the address buffers are hardwired to the one address bus and all the data latches are hardwired to the one data bus. This means that enable and select pulses must be generated at proper times to insure required data separation and organization. The timing scheme used to accomplish this is described in the following paragraphs. Constant reference to figure 11, the master timing chart for DIU functioning, will be made. Figure 11 illustrates the sequence of events required for one read/write cycle which is repeated until all data words are transferred.

Data Read/Write Sequence:

Starting at the upper left of figure 11, there are a series of pulses proceeding diagonally down the chart. It is these pulses that control the specific word of the specific bus that is to be read at any instant. It is seen that there are two word transfers for each bus word and for each return word. This is because a SIR location is 16 bits and each SPRP word contains 32 bits; thus two SIR locations are required for storage of each display bus SPRP word. The sequence of data transfer is shown in the left column of figure 11. At the end of the marked 16 microsecond interval, both SIR locations of each display SPRP input bus word and both SIR locations of a return SPRP word have been transferred.

SIR Access Control:

Since the SIR is shared by the DIU and the DATAC bus, there must be times when each device has control. This is accomplished by generation in the DIU of the ADDRESS STROBE signal shown in figure 11. This is a periodic square wave with a period of 2 microseconds (one microsecond high and one

microsecond low). While this signal is low the DIU can read from and write into the SIR location whose address it places on the address bus; while it is high the DATAC terminal has control of the SIR. Looking at the top left of figure 11, it is seen that the pulse corresponding to the READ BUS 1, WORD 1 condition goes low (its active state) while the ADDRESS STROBE is high (T1). This assures that the desired address will be ready and settled on the address bus when the ADDRESS STROBE goes low. Then when the ADDRESS STROBE goes low (T2 in figure 11), Bus 1 address latches are enabled thus granting control of the address bus to whatever Bus 1 address the latches contain. This constitutes a request for the SIR to allow a read of the data in the addressed location. This condition will exist until the READ BUS 1, WORD 1 again goes high (just beyond T3 in figure 11) at which time a Bus 2 address obtains control of the address bus. As the cycle continues, every required address will get its turn on the address bus.

Specific Data Word Read Time:

Once the data request conditions of the last paragraph occur, the SIR requires one more signal before it allows data from the requested location be used. This is the DATA STROBE shown in figure 11. The DATA STROBE is a low active signal generated by the DIU and occurring during the low active time of the ADDRESS STROBE. It is during DATA STROBE active time that the DIU is assured of finding valid settled data in the addressed SIR location. The DIU DATA LATCH PULSE is generated during the DATA STROBE pulse time and is used to effect actual data capture. Data bits from the addressed SIR location are actually latched on the falling edge of this DATA LATCH PULSE which must occur before the end of the active (low) time of the DATA STROBE pulse. In order to allow maximum settling time for SIR data, this falling edge is made to occur near the end of the DATA STROBE pulse active time, T3 in figure 11. The same cycle is repeated twice more to read the first 16-bit SIR locations of Busses 2 and 3, up until time T4 in figure 11. At T4 the first 16 bits of the first return SPRP word are written into the proper SIR location by the DIU. Examination of figure 11 shows that the READ/WRITE control signal also goes low at time T4. The READ/WRITE control signal is generated in the DIU and determines whether the addressed SIR location is to be read from or written into. When the READ/WRITE control pulse is high, only a read can occur; when it is low the DIU can write into the addressed SIR location. Thus it is necessary for the READ/WRITE pulse to be low during the writing time of the return words.

After this DIU write operation data for the first 16-bit SIR location of each pertinent SPRP data word have been transferred. The DIU then generates the STEP COUNTER pulse for incrementing to the next location. All active counters respond to this signal and are incremented at its falling edge, time T6 in figure 11. From this point, the cycle described above is repeated until all required SIR locations are addressed. As has been discussed previously, each counter will independently reset itself when its preset

maximum count is reached. Once reset the counter will ignore all step counter pulses (refuse to cycle) until the logic shown in figure 3 is again satisfied. Also once a counter is started it will not stop in response to any external control pulses until its maximum count is reached.

SPRP Transmitter Timing Control:

The SPRP transmitter start pulses are shown at the bottom of figure 11 and occur at times T7, T8, and T9. Examination of the Bus 1 start pulse (T7) shows that it occurs slightly before the end of the READ BUS 1, WORD 2 control pulse (near the center of the diagram) and simultaneous with the falling edge of the DIU DATA LATCH PULSE which captured data from the second bus 1 SIR location. At this time both 16-bit words of the Bus 1 32-bit SPRP word have been read from the SIR and their data enabled in the DIU data latches. The SPRP data word is then ready for transmission to the display system, a task accomplished by starting the transmitters which read the data latches bit by bit, convert the TTL data to SPRP pulse configuration (figure 3), and send it serially to the receivers in the display system input circuitry.

Further examination of figure 11 shows that the two other busses are treated identically at times T8 and T9, respectively, when the second word of each of these busses has been read and latched. Latching of return word data into SIR buffers is accomplished by SIR supporting circuitry and thus no action by the DIU is required for this function.

Circuitry for Time Control Pulse Generation:

The circuitry used to generate the timing control signals of figure 11 is illustrated in figure 12. A 2 Mhz master clock is used as a reference for all time functions. The READ/WRITE control signals for individual bus words are generated from a 2716 EPROM whose addressing is controlled by a counter circuit composed of 54LS193 chips. Counter outputs are EPROM addresses which are created via a clock derived counter input. In the absence of an active address input, all EPROM output lines are high. When an active EPROM address occurs, a low state results for one corresponding output line which in turn constitutes a word read or write select signal. As the EPROM addresses are serially cycled, the series of low active pulses beginning at the top left of figure 11 result. Only one line will be low at any specific time insuring that each necessary address location is allocated its own unique time on the address bus. The data latching method previously discussed insures capture of the contents of each location when its value is active on the address bus. Figure 12 also illustrates the method used to insure a default address of 0600H (bus control word address) on the address bus. It is seen in figure 12 that all the READ/WRITE control signals are input into a 54LS30 NAND gate. While all these lines are high the output of the NAND gate is low, thus activating the gate and latching the fixed input

address value onto the SIR address bus. This fixed input address is 0600H which is the location of the bus control word. When any one of the NAND gate inputs goes low, the gate output is disabled thus allowing the line which is low to control the address value. Since the default state of all EPROM output lines is high, the default address will reside on the address bus anytime an EPROM address does not select an output read or write operation.

Read/Write Control Pulse Generation:

The READ/WRITE control pulse discussed above in connection with figure 11 is generated by directing the write control pulses into a 54LS08 AND gate (Gate 1, figure 12). Since these lines are normally high the AND gate output will be high (read state) except when either write control line goes low. Then the AND gate output will become low which is the write state and the DIU can write into the SIR. This corresponds to the above discussion of the pulse timing shown in figure 11 where it is seen that the WRITE RETURN WORD pulse and the READ/WRITE control pulse are simultaneously low. The STEP COUNTER pulse is generated by the logic AND of the inverted READ/WRITE control pulse and the inverted ADDRESS STROBE PULSE as illustrated in the lower center of figure 12, Gate 2. Since the READ/WRITE control pulse is high for reading, its inverted state holds Input 1 to Gate 2 low during all read times. When the DIU issues a write request the READ/WRITE pulse goes low thus bringing Input 1 to Gate 2 high. Then, upon the next occurrence of a low state of the ADDRESS STROBE, Input 2 to Gate 2 (inverted ADDRESS STROBE) goes high and thus the output of Gate 2 becomes high generating the STEP COUNTER pulse. Examination of figure 11 shows this event; the STEP COUNTER pulse occurs simultaneous with low READ/WRITE and ADDRESS STROBE pulses. The duration of the STEP COUNTER pulse is only the low time of the ADDRESS STROBE (1 microsecond) because, as seen in figure 11, both the READ/WRITE and ADDRESS STROBE pulses go high again.

Address and Data Strobe Generation:

ADDRESS STROBE and DATA STROBE signals are generated as illustrated in figure 12. The ADDRESS STROBE is a continuous 0.5 Mhz signal obtained by dividing the 2 Mhz clock by 4. This division is accomplished by use of the appropriate stage of the EPROM address counter. The DATA STROBE must be delayed slightly after start of the ADDRESS STROBE (figure 11 and previous discussion). A monostable multivibrator (54LS123) with suitably adjusted timing networks is used to produce this pulse with the proper delay and duration. The input pulse to the 54LS123 is the ADDRESS STROBE as shown in figure 12 thus insuring that no DATA STROBE will occur until the ADDRESS STROBE exists. Once created the DATA STROBE duration is controlled by a 54LS123 timing network so that it ends slightly before the end of the ADDRESS STROBE pulse which initiated it. The timing required is illustrated in figure 11 and was discussed previously.

Physical Flight Configuration:

The installation configuration of the TSRV display system is shown in figures 13 and 14 which are photographs of the actual flight equipment racks. Figure 13 shows the ADEDS display generation flight equipment which consists of the display processor, the digital-to-analog unit for production of deflection and video signals, and monitoring units used for system operation and maintenance. Except for the computer terminal at the top left this rack of equipment remains the same as in the previous TSRV experimental system. Figure 14 shows the installation of the new components, the DII, and its associated DATAC terminal. These two display-related units are mounted in the flight management rack across the aircraft aisle from the display equipment shown in figure 13, an arrangement made necessary to avoid overcrowded conditions near the egress passage directly behind the research flight deck.

CONCLUDING REMARKS

The Display Interface Unit (DIU) was designed, constructed, tested, and installed in the upgraded TSRV experimental flight system for interfacing the original TCV monochrome display system (ADEDS) to the new DATAC serial data bus. A unique design was necessary to satisfy the ADEDS data interface requirements of three input SPBP serial data busses and one output SPBP bus.

The resulting DIU has been fully tested in the TSRV operational environment, and its performance has satisfied all design criteria. It is expected to readily perform satisfactorily until a new color display system is installed in the TSRV, at which time the monochrome ADEDS will no longer be used.

REFERENCES

1. Herzog, H. K.: Commercial Airplane Data Bus Requirements and DATAC. SAF-A-2K High Speed Data Bus Subcommittee, Dayton, Ohio, WPAFR/ASD, May 22, 1981.
2. Easley, Wesley C.; Lynn, William A.; and McLeur, David G.: Improved Memory Loading Techniques for the TSRV Display System. NASA Technical Memorandum 87649, Langley Research Center, January 1986.

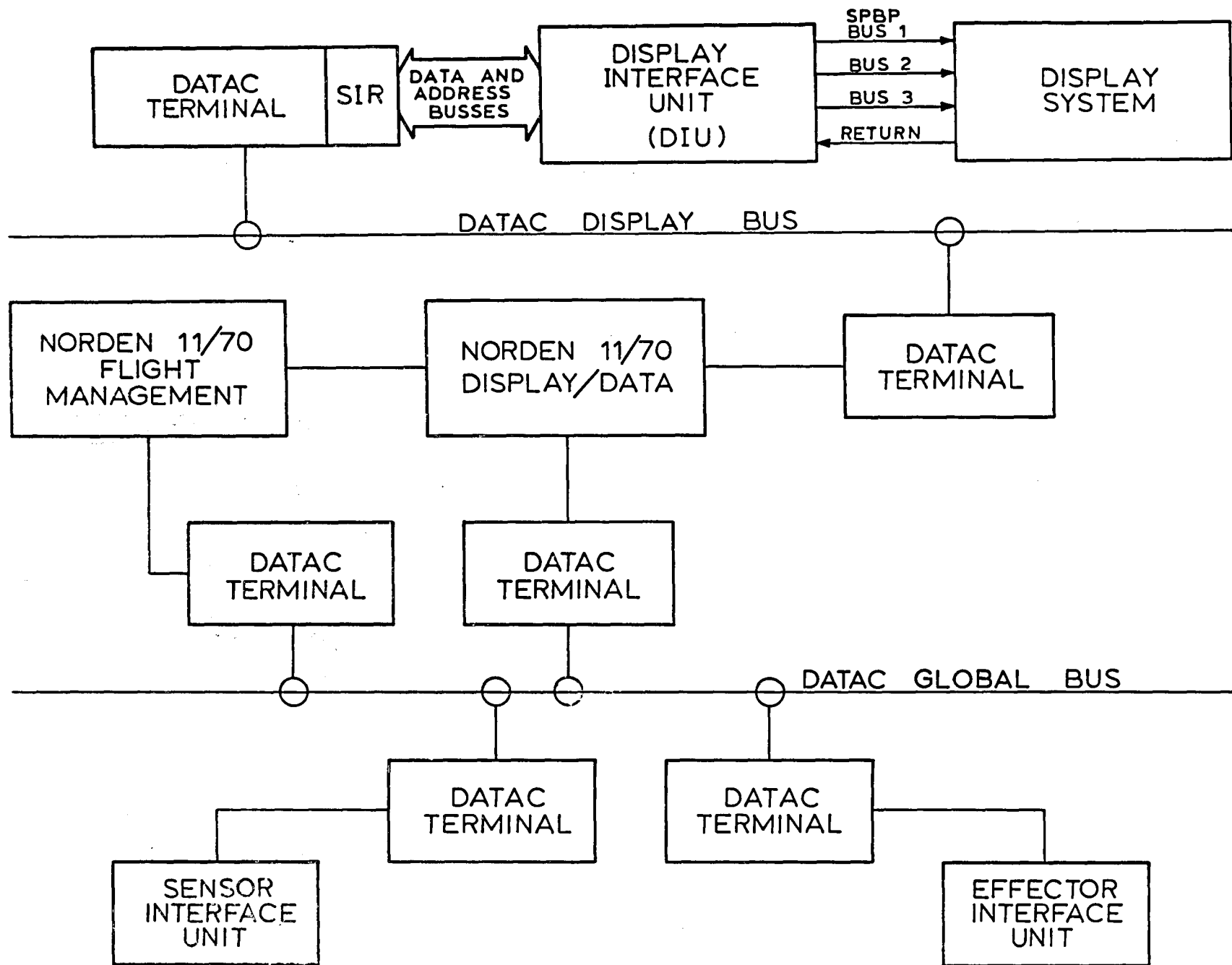


FIGURE 1. TSRV UPGRADE STRUCTURE

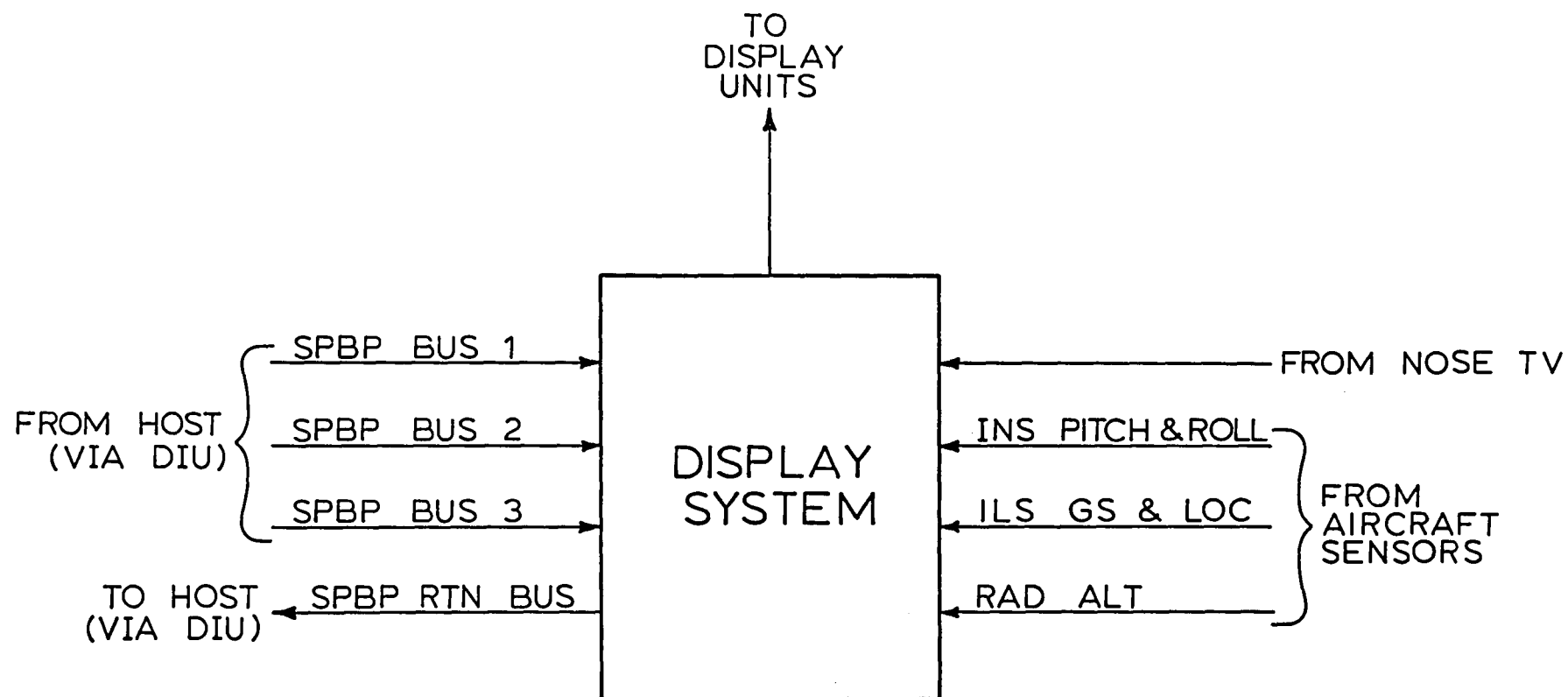


FIGURE 2. DISPLAY SYSTEM INTERFACE SIGNALS

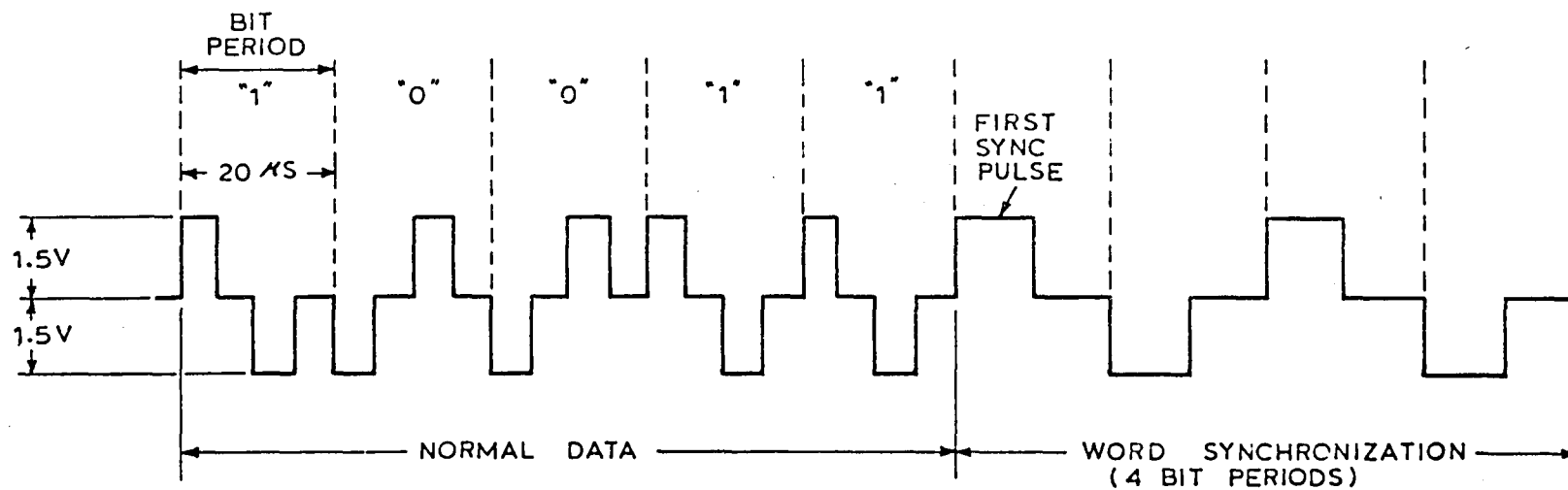
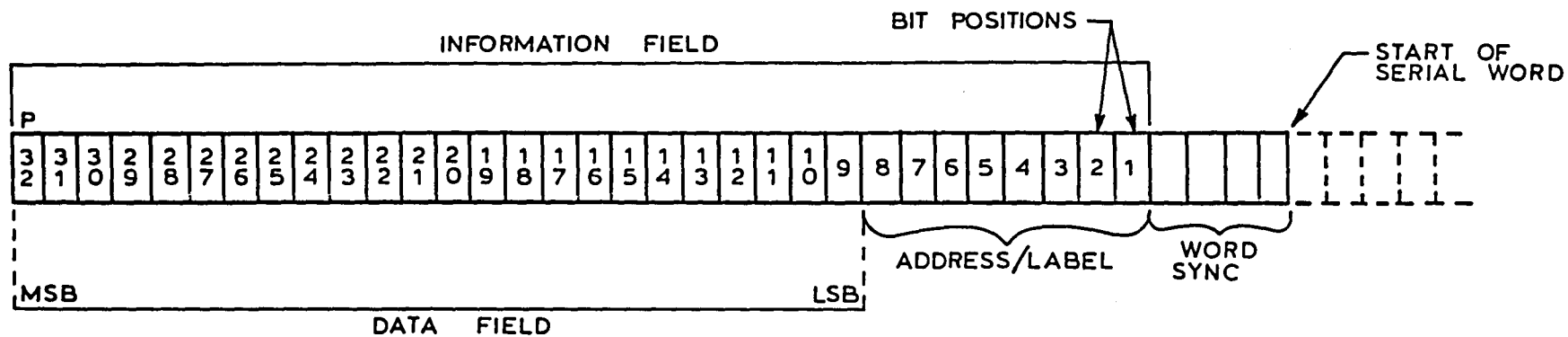


FIGURE 3. SPBP TRANSMISSION LINE WAVEFORM



18

NOTE:

P = PARITY

FIGURE 4. SPBP WORD STRUCTURE

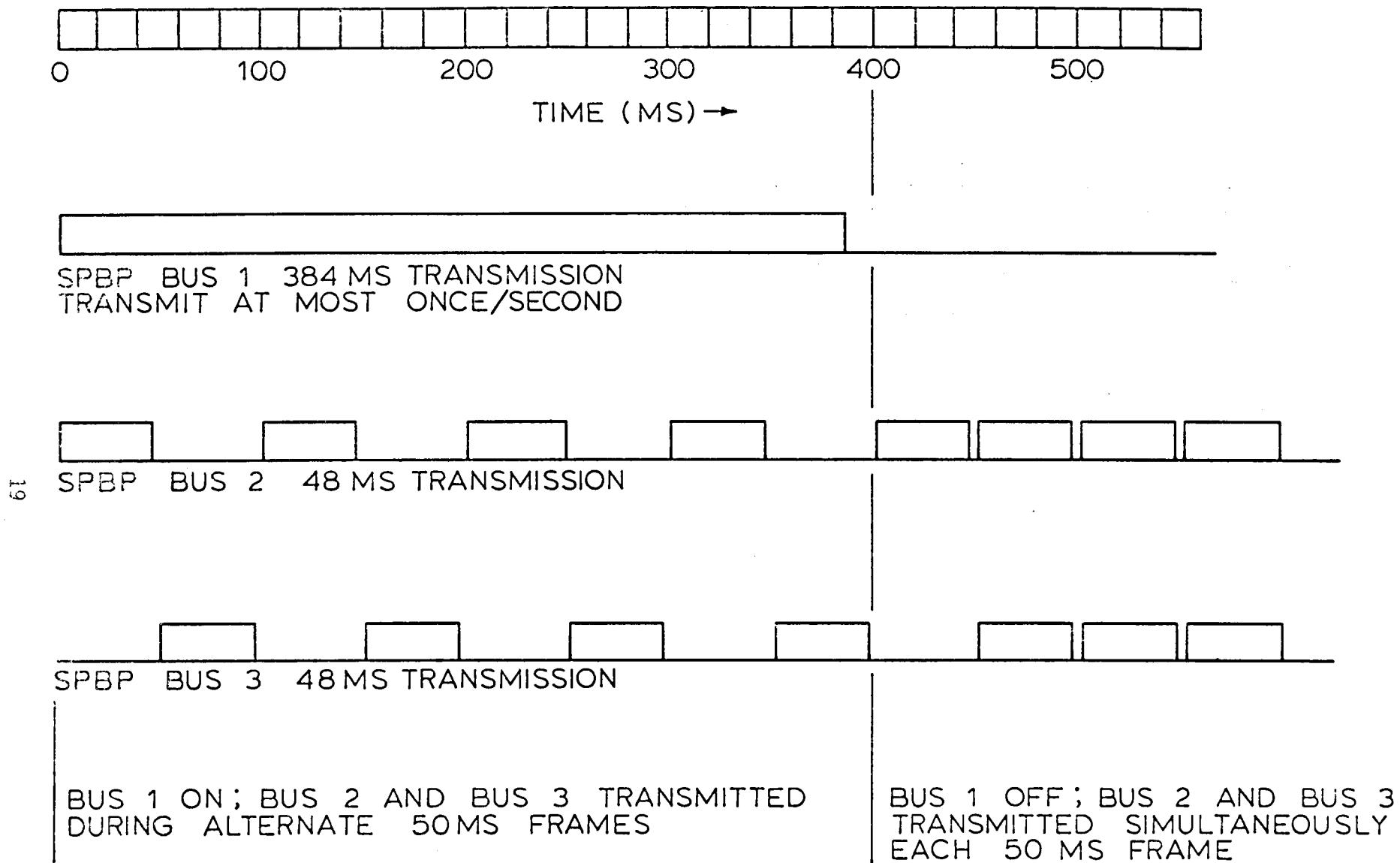


FIGURE 5. DISPLAY INPUT BUS TRANSMISSION TIMING

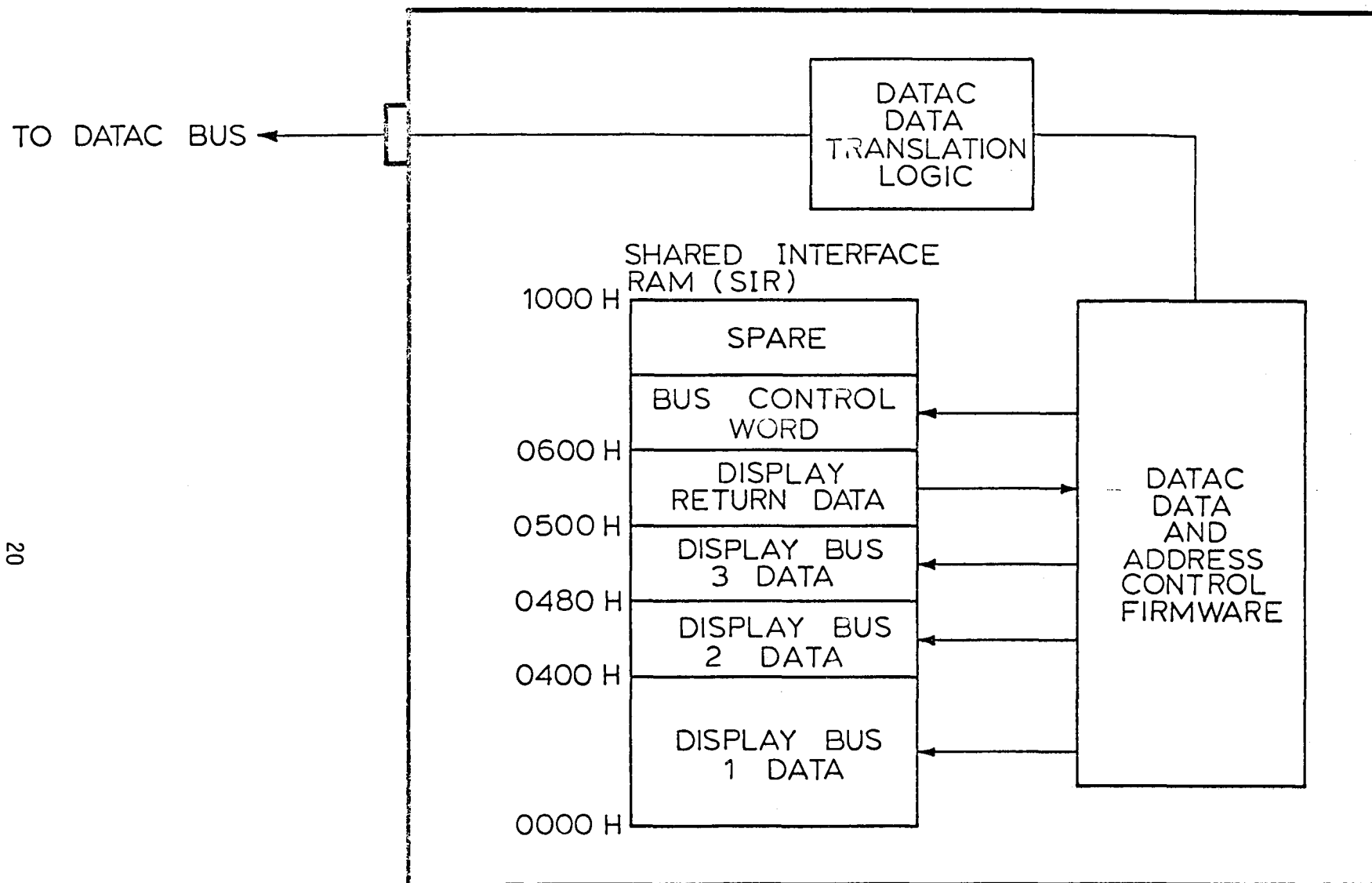


FIGURE 6. DATAC TERMINAL AND SIR ARRANGEMENT

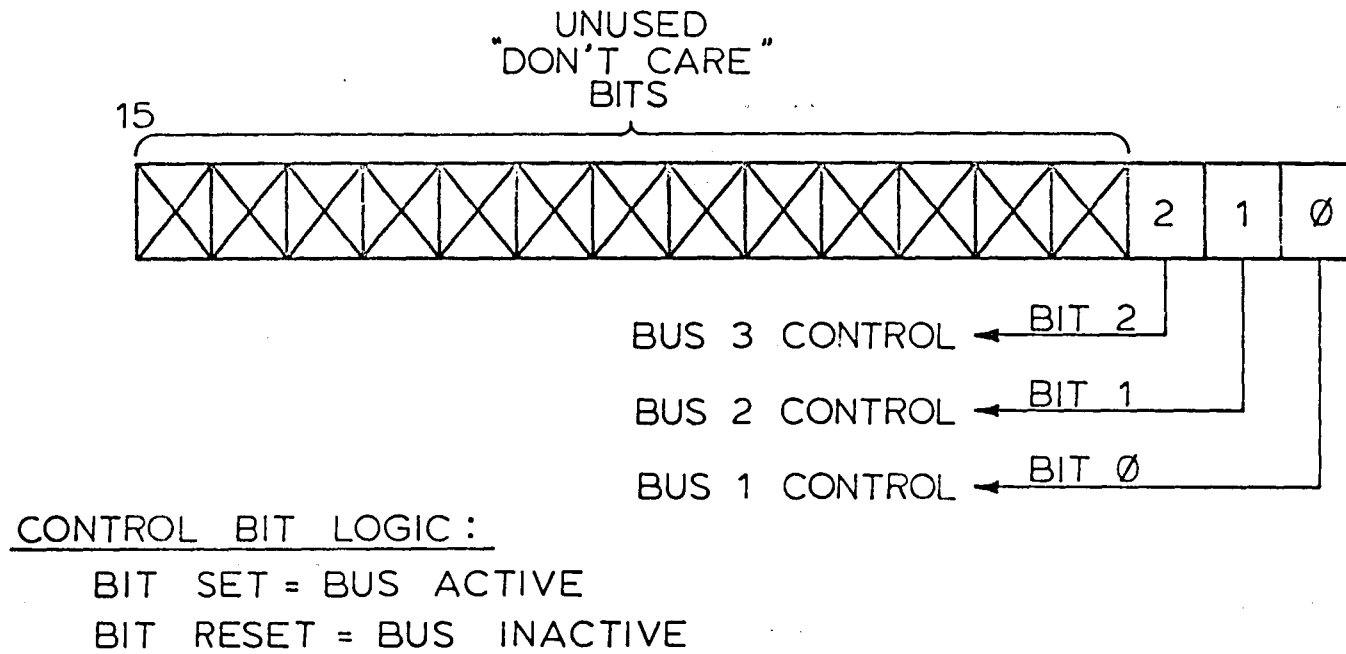


FIGURE 7. DISPLAY INPUT BUS CONTROL WORD STRUCTURE

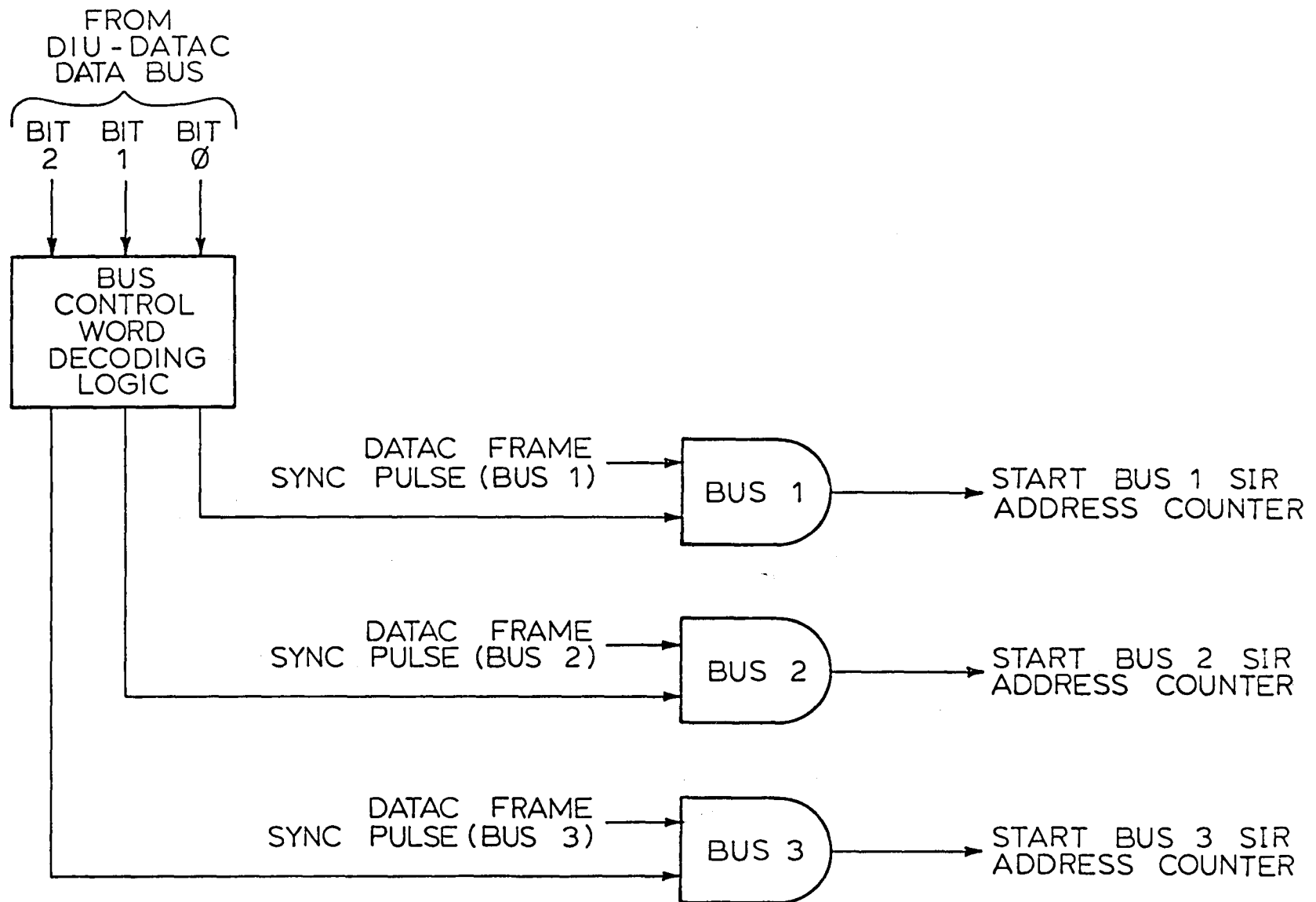


FIGURE 8. DATAC/NORDEN/DIU SYNCHRONIZATION METHOD

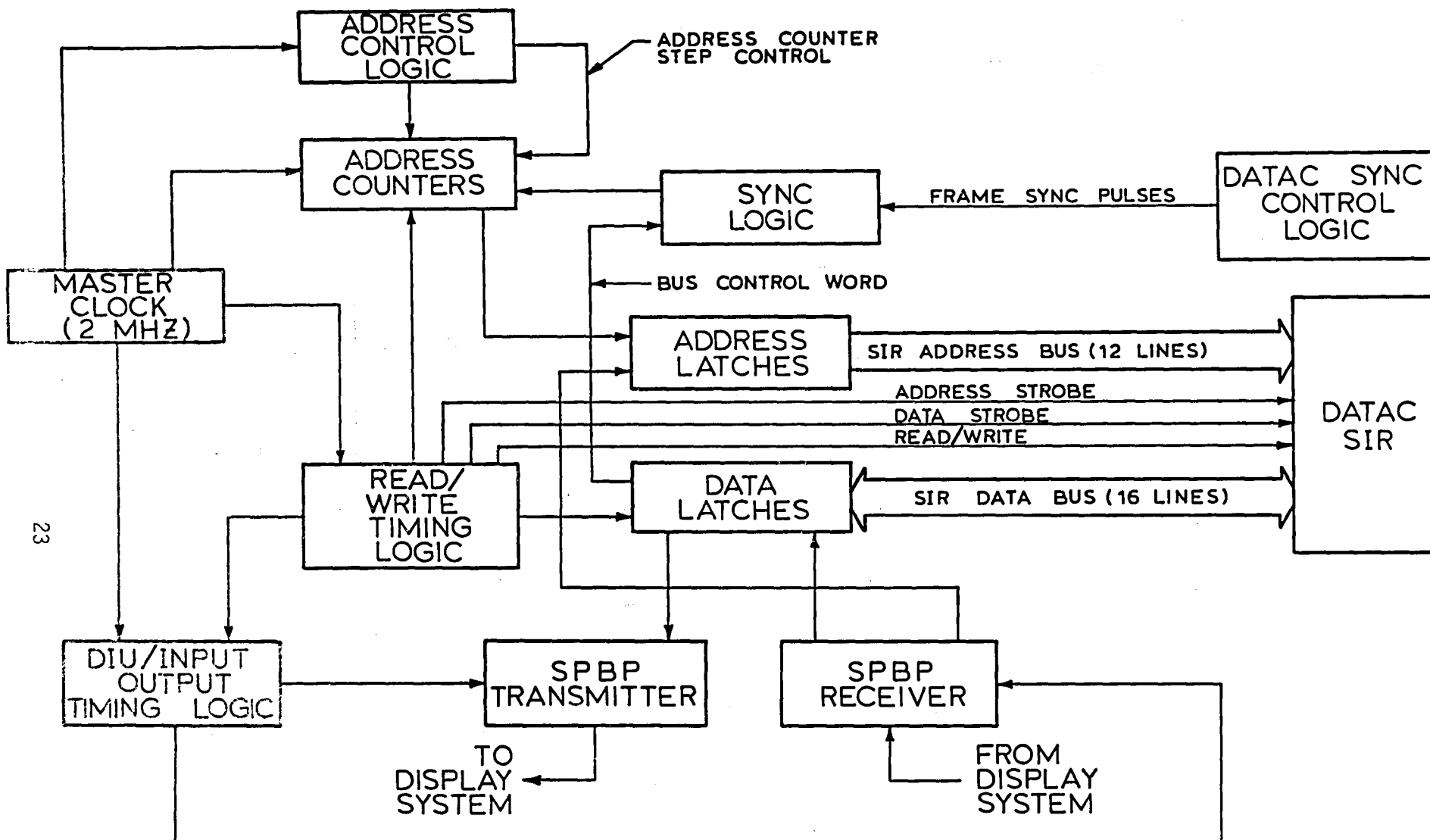


FIGURE 9. DIU FUNCTIONAL DIAGRAM

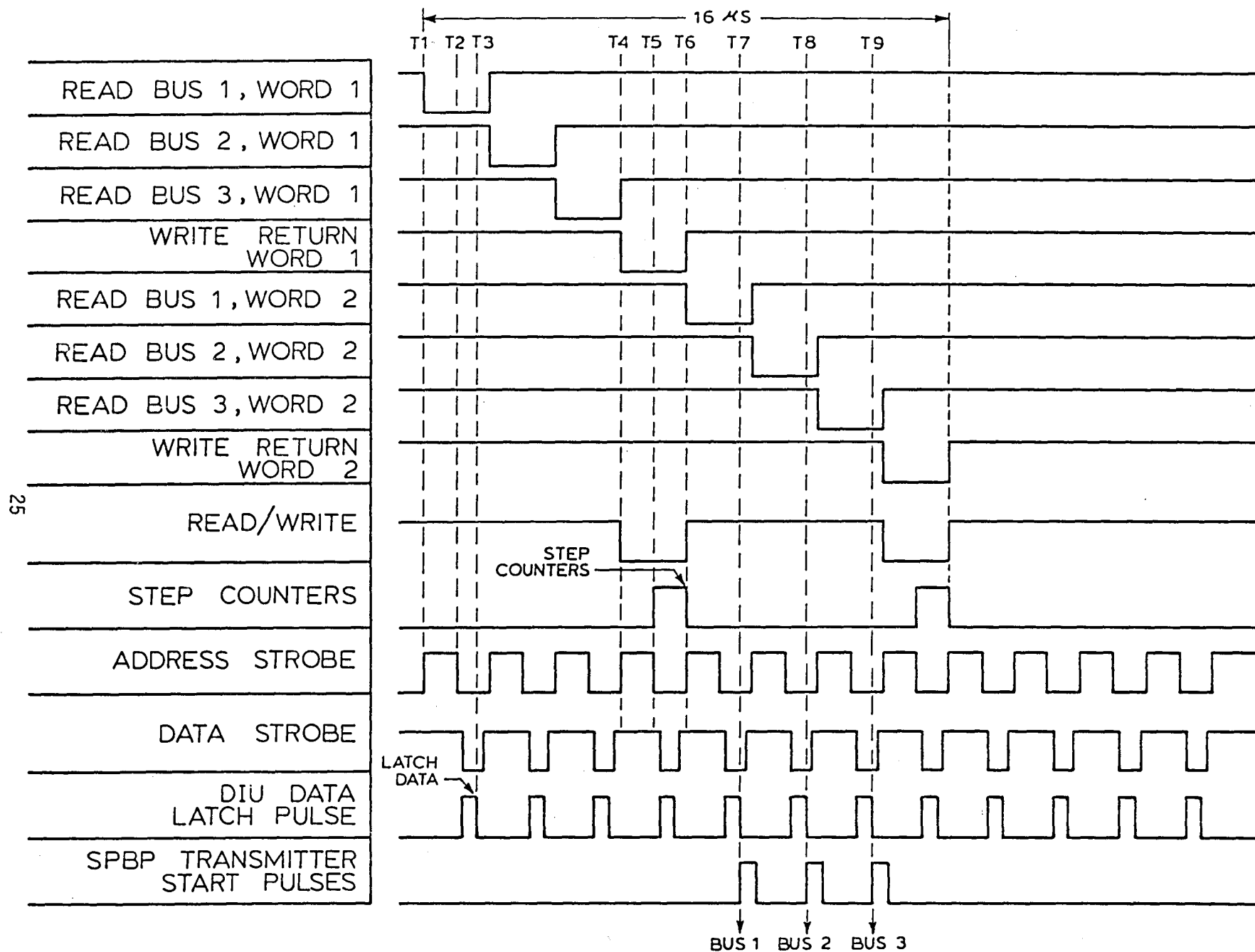
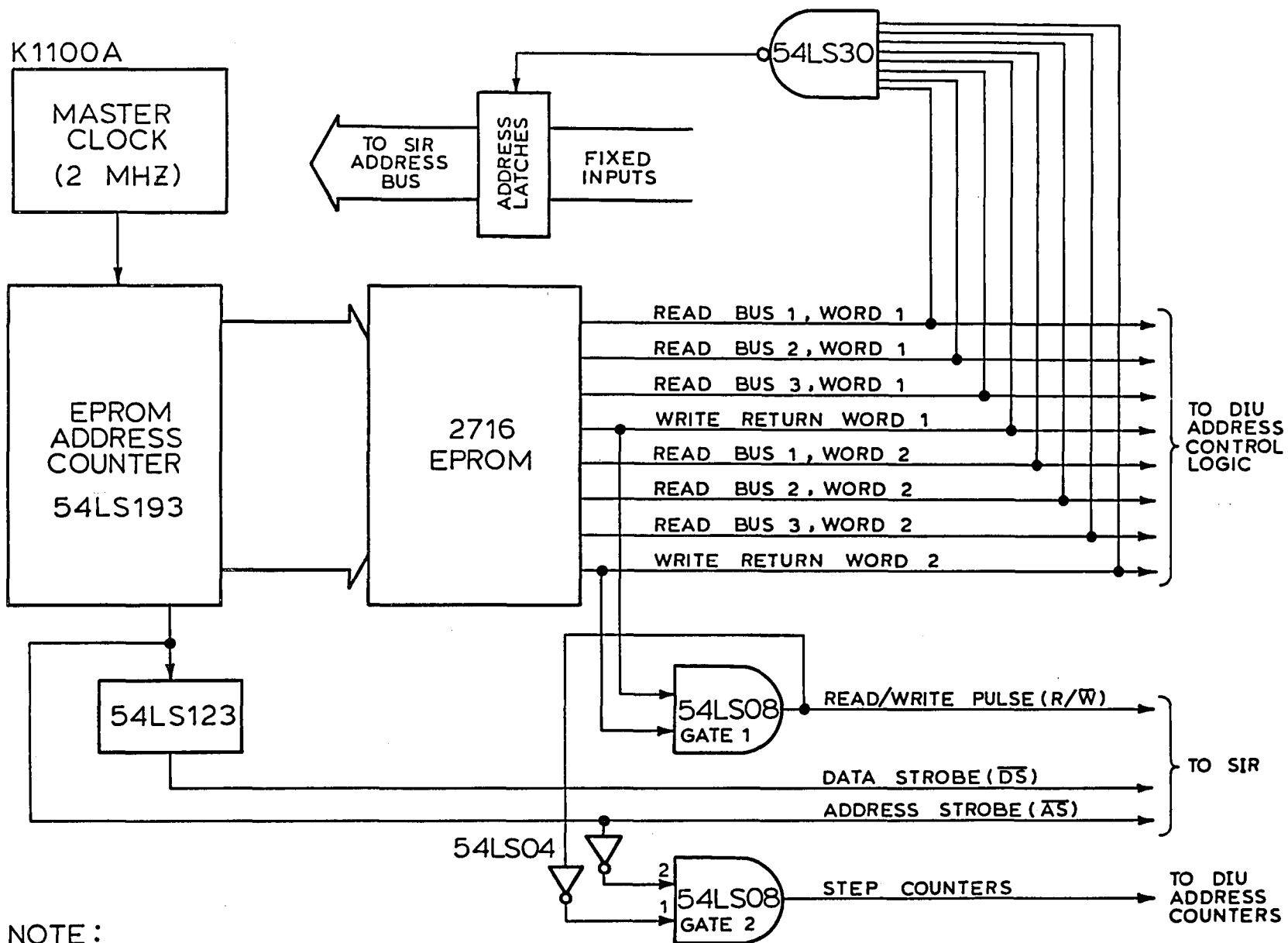


FIGURE 11. DIU READ/WRITE TIMING CHART

**NOTE:**

ALL SIGNALS SHOWN
ARE ACTIVE LOW.

FIGURE 12. - GENERATION IN DIU OF DATA TRANSFER CONTROL SIGNALS.

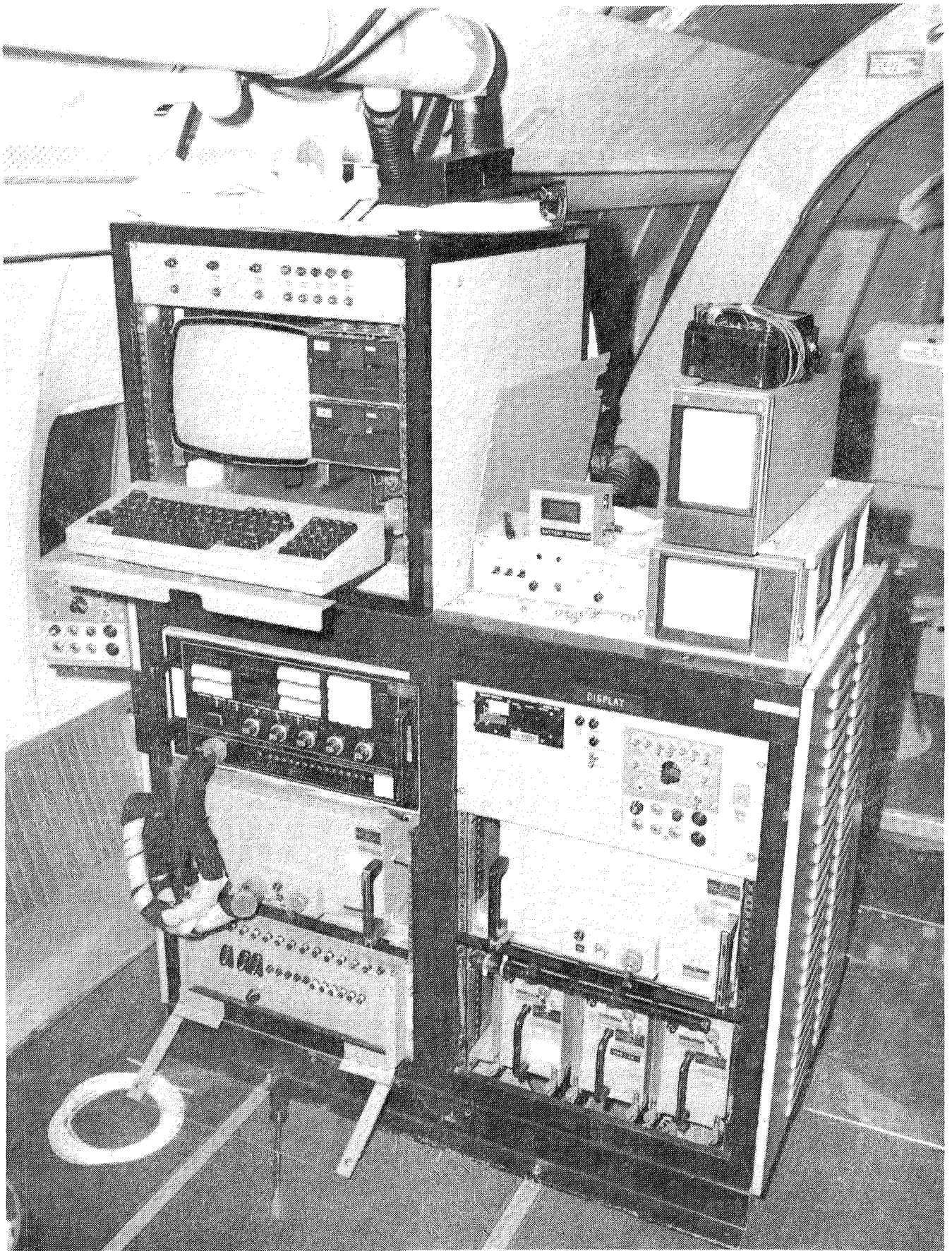


Figure 13. AEDS Flight Equipment

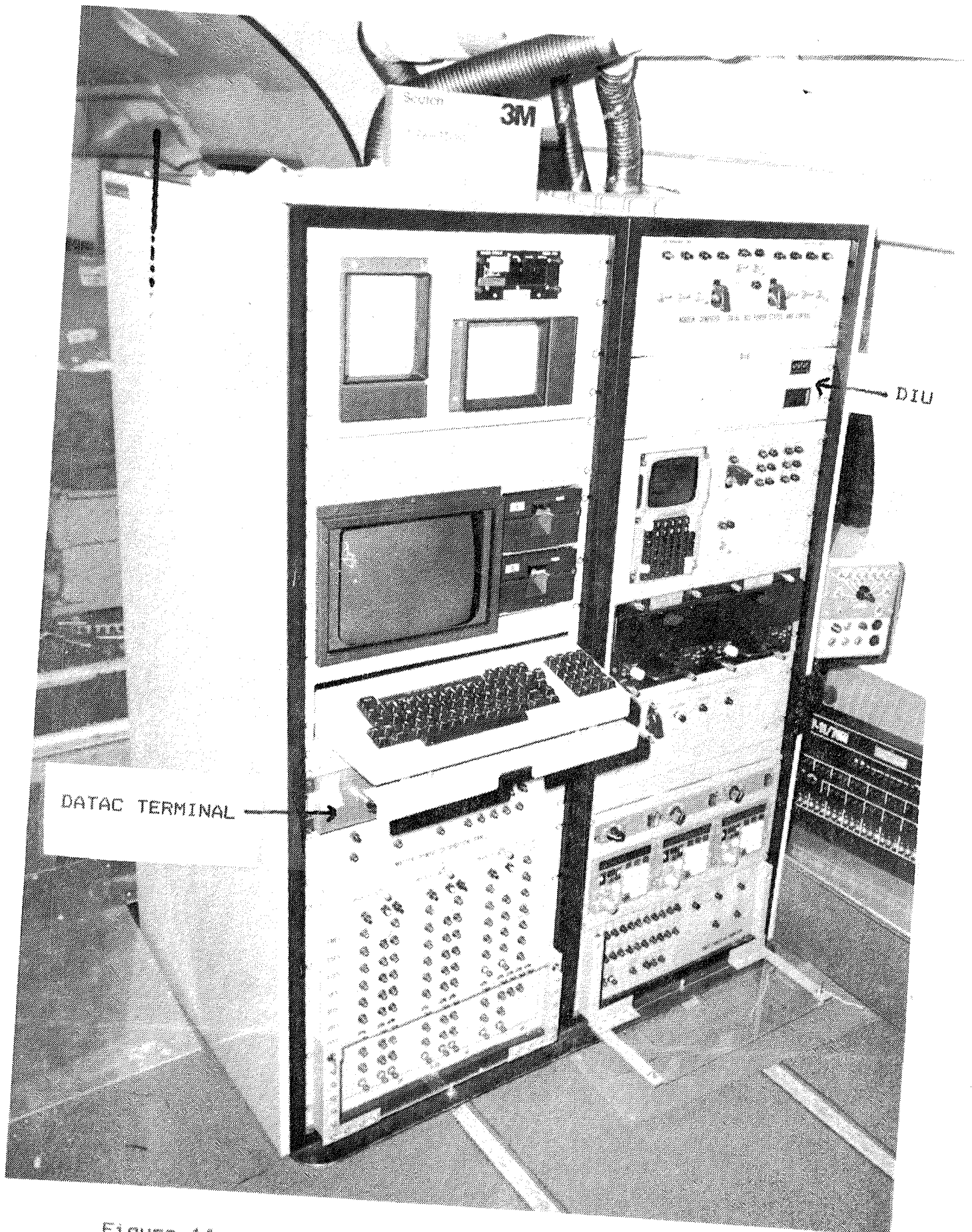


Figure 14. DIU and DATAC Terminal Flight Installation

Standard Bibliographic Page

| | | | | | |
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| 16. Abstract A recent upgrade of the Transport Systems Research Vehicle (TSRV) experimental flight system at the NASA Langley Research Center retained the original monochrome display system. However, the original host computer was replaced with a Norden 11/70, and a new Digital Autonomous Terminal Access Communication (DATA) data bus was installed for data transfer between display system and host. Thus, a new data interface method was required. The display data interface makes use of four Split Phase Bipolar (SPBP) serial busses. The DATA bus used a Shared Interface Ram (SIR) for intermediate storage of the data it transfers. A unique Display Interface Unit (DIU) was designed and configured to read from and write to the SIR and properly convert the data from parallel to SPBP serial and vice versa. Separation of data for use by each SPBP bus and synchronization of data transfer throughout the entire experimental flight system were major problems requiring solution in DIU design. This paper describes the techniques used to accomplish these new data interface requirements. | | | | | |
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